GRADE A

MESC TECHNICAL NEWS

No. M7700-61-9912

Corrections and Supplementary Explanation for "7700 Family Software Manual" (REV.D)

This news includes a few corrections and supplementary explanation for "7700 Family Software Manual".

And also, this news includes the information previously announced by the MESC TECHNICAL NEWS (No. M7700-32-9803, Corrections and Supplementary Explanation for "7700 Family Software Manual" REV. C). ★ represents the new information.

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- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcomputer Development Support Tools (http://www.tool-spt.mesc.co.jp/index_e.htm)

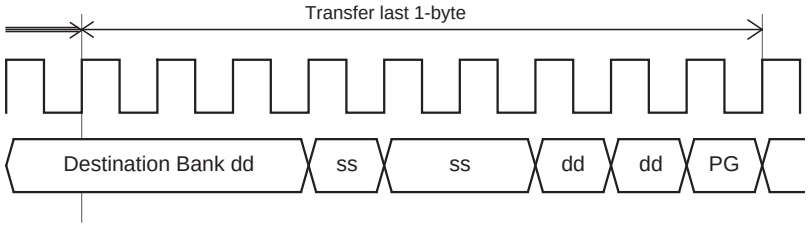
Corrections and Supplementary Explanation in “7700 Family Software Manual” (REV.D) No.1

Page	Error	Correction
P2-7 (2) Zero flag (Z)	**Note**: This flag has no meaning in decimal mode addition (the **ADC** instruction).	**Note**: This flag has no meaning in decimal mode addition (the **ADC** instruction) and subtraction (the **SBC** instruction).
P4-10 **ADC** **[Status flags]**	C: When the data length selection flag m is set to 0, set to 1 if binary addition exceeds +65535 or if decimal addition exceeds +9999. Otherwise, cleared to 0. When the data length selection flag m is set to 1, set to 1 if binary addition exceeds +255 or if decimal addition exceeds +99. Otherwise, cleared to 0.	C: If unsigned binary addition is performed, set to 1 in the cases as follows; ● the case when the result of addition exceeds +65535 with data length selection flag m = 0. ● the case when the result of addition exceeds +255 with data length selection flag m = 1. Otherwise, cleared to 0. If unsigned decimal addition is performed, set to 1 in the cases as follows; ● the case when the result of addition exceeds +9999 with data length selection flag m = 0. ● the case when the result of addition exceeds +99 with data length selection flag m = 1. Otherwise, cleared to 0.
P4-34 **CMP**, P4-35 **CPX**, P4-36 **CPY** **[Status flag]**	C: Set to 1 if the result of operation is 0 or larger. Otherwise, cleared to 0.	C: If unsigned operation is performed, set to 1 when the result of operation is 0 or larger. Otherwise, cleared to 0.
P4-40 **DIV** **[Status flag]**	I: Not affected.	I: Not affected. ✻Set to 1 when divisor is 0.

Corrections and Supplementary Explanation in "7700 Family Software Manual" (REV. D) No.2

	Page	Error	Correction
★	P4-86 **PSH** **[Operation]**	M(S to S – n) ← A, B, X, Y, DPR, DT, PG, PS order to save ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ S ← S – n – 1	M(S to S – n + 1) ← A, B, X, Y, DPR, DT, PG, PS order to save ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ S ← S – n
	P4-96 **SBC** **[Status flags]**	Z: Set to 1 when the result of operation is 0. Otherwise, cleared to 0. C: Set to 1 when the result of operation is equal to or larger than 0. Otherwise, cleared to 0, and a borrow is indicated.	Z: Set to 1 when the result of operation is 0. Otherwise, cleared to 0. Meaningless for decimal subtraction. C: If unsigned operation is performed, set to 1 when the result of operation is equal to or larger than 0. Otherwise, cleared to 0, and a borrow is indicated.
★	P4-129 (2)	(2) The program bank register •••	(2) As for the products with the internal ROM area consisting of 60 Kbytes or less, the program bank register •••
	P4-129 (3)	(3) When "1" is set in the D-flag for decimal operation: The C-flag alone is effective in the **ADC** instruction, while the Z, N and V flags are disabled. The C and Z flags alone are effective in the **SBC** instruction, while the N and V flags are disabled.	(3) When "1" is set in the D-flag for decimal operation: The C-flag alone is effective in the **ADC** and **SBC** instructions, while the Z, N and V flags are disabled. (Delete)
	P6-2 Line 3 under the table	: : B, and an internal processing cycle added at the front. (See the figure in the next page.) The number of φCPU cycles differs in the : :	: : B, and an internal processing cycle added at the front. (See the figure in the next page.) However, even when accumulator B is used, the number of cycles required in the **ASR**, **EXTS**, and **EXTZ** instructions are the same. The number of φCPU cycles differs in the : :
	P6-46	Timing:  	Timing: 

Corrections and Supplementary Explanation in “7700 Family Software Manual” (REV.D) No.3

Page	Error
P6-85 **MVP**	Timing: ●The transfer of odd byte (the last cycle of the second timing chart) 
	Correction
	Timing: ●The transfer of odd byte (the last cycle of the second timing chart)