- System LSI -

32 bit ARM based RISC MPU

FOCUSING GUIDE v2.1x

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I. SAMSUNG'S ARM FAMILY

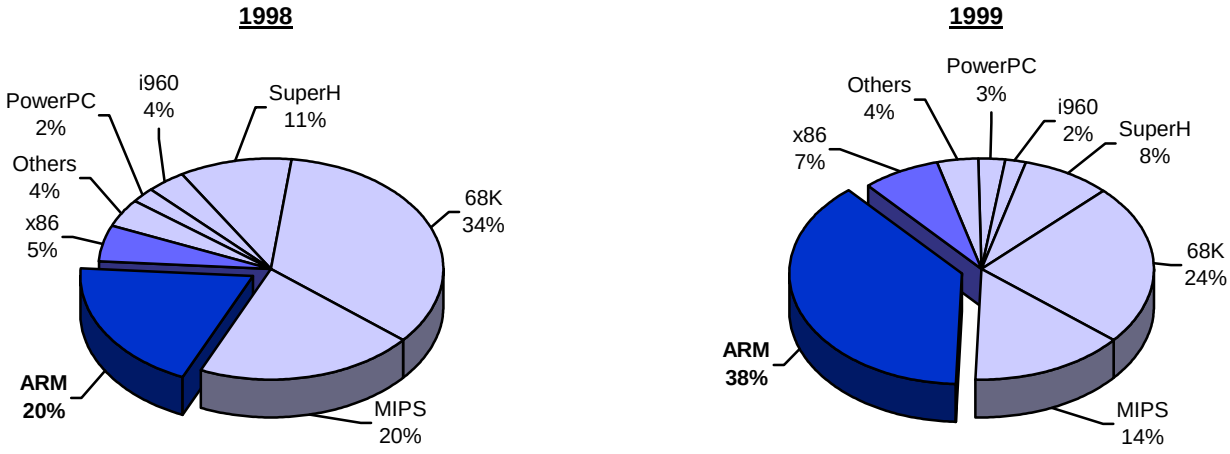
A. ARM architecture

In the 80's, on an opposite way from the competitors (Intel, Motorola and so on), Advanced RISC Machines (ARM) designed an outstanding CPU cores family based on following rules :

1. Efficiency
2. Reliability
3. Simplicity

The goal was to define an architecture that joined on one hand a high power of treatment and on the other a low consumption.

Nowadays, ARM is offering a concept and a family of CPU cores using by the world-wide majors semiconductors companies. We can find ARM CPU cores in a growing number of embedded systems that claim more and more power such as mobile phones, notebooks.



The range of ARM's cores begins with the ARM7TDMI to continue with ARM9 and ARM10. This is more different versions, but they are not the topic of this note.

For more information, you can visit ARM website at www.arm.com.

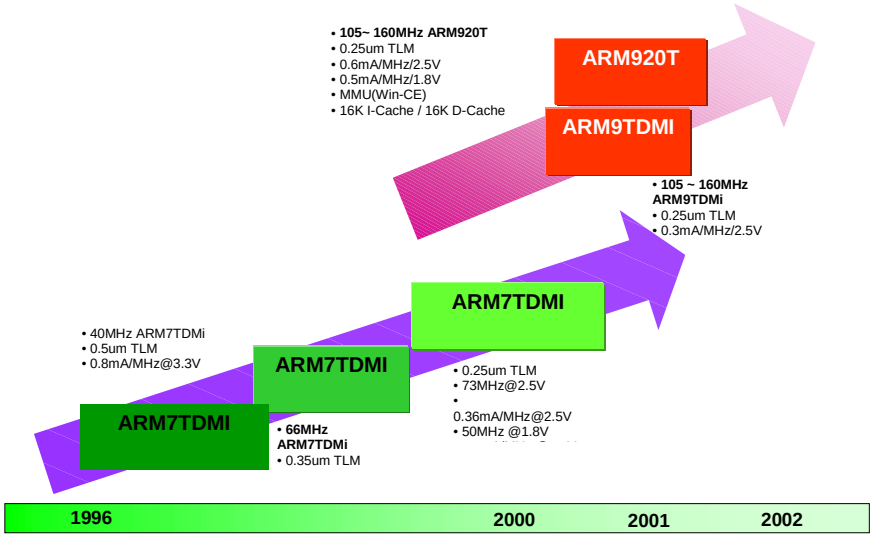
B. ARM7TDMI, ARM9TDMI cores

These cores implement the Thumb instruction set and an in circuit debug mode (TDMI = "Thumb and Debug Mode In circuit).

The Thumb instruction set is an extension of the 32 bits ARM architecture. Thumb instructions are a subset of the most commonly used 32 bits ARM instructions which have been compressed into 16 bits opcodes. On execution, these 16 bits instructions are decompressed to 32 bits ARM instructions in real time without performance loss. The use of Thumb code provides typical memory savings of 35-40%.

An Embedded ICE unit is also implemented to provide code-download, hardware break-pointing and semi-hosting I/O. Access is via a 5 wires JTAG port and an interface such as ARM's Multi-ICE unit.

Below, we can see the roadmap planned by Samsung :



Actually, SAMSUNG is using the ARM7TDMI core and the ARM9 is planned for Q4 2001.

C. The tools

A complete range of development tools exist :

- ARM SDT : provides a complete software development solution.
  C compiler, Assembler, Linker & Thumb instruction set, a Simulator, Debugger …
- Multi ICE : is a powerful JTAG based in-circuit emulator (ICE) that enables the non-intrusive debug of embedded processors at full speed.
- Evaluation boards based on different SAMSUNG processors (see beyond)
- An now, with have a partnership with WindRiver for a complete toolchain offer !

II. COMMUNICATIONS SOLUTIONS

A. Overview

For communication solution, like internet appliances, SAMSUNG is offering low-cost and powerful components.

Several main interfaces are present :

1. **Ethernet**
2. **Modem**
3. **ATM SAR**

B. Main communications components

1. Ethernet controller

The Ethernet controller operates at either **100-Mbits** or **10-Mbits** per second :

- In half-duplex mode, supports the IEEE 802.3 carrier sense multiple access with collision detection (CSMA/CD) protocol.
- In full-duplex mode, supports the IEEE 802.3 MAC control layer, including the pause operation for flow control.

The Ethernet controller's MAC layer supports both the media independent interface (**MII**) and the buffered DMA interface (**BDI**). The MAC layer itself consists of the receive and the transmit blocks, a flow control block, a content addressable memory (CAM) for storing network addresses, and a number of command, status, and error counter registers.

The MII supplies the transmit and receive clocks of 25 MHz for 100-Mbit/s operation or 2.5 MHz at the 10-Mbit/s speed. The MII conforms to the **ISO/IEC 802-3** standards for a media-independent layer that separates physical layer issues from the MAC layer.

2. HDLC (High-level Data Link Controller)

HDLC controller is doing for serial communications.

The HDLC module supports a CPU/data link interface that conforms to the synchronous data link control (**SDLC**) and high-level data link control (**HDLC**) standards.

In addition, the following function blocks are integrated into the HDLC module:

- Two-channel DMA engine for Tx/Rx
- Support buffer descriptors per frame
- Digital phase-locked loop (DPLL) block
- Baud rate generator (BRG)

3. SAR / UTOPIA interface

The Segmentation And Reassembly module (SAR) is for providing packet to ATM connectivity. Once a data packet is given to the SAR, it is translated into cells using either the AAL5 protocol or the null AAL protocol. Then, without further host intervention, the cells are transmitted using selected scheduling algorithms. The host is notified upon completion of the packet transmission. The SAR also receives cells from the PHY device, reassembles them into packets, and notified the host when a packet has arrived.

The Universal Test and Operations PHY Interface for ATM (UTOPIA) is for receiving and transmitting ATM cells.

C. The offer

5 parts are mainly existing for Ethernet-based systems :

- **S3C4510B01** for Ethernet Appliances,
- **S3C4530A**, a pin-to-pin compatible upgrade of S3C4510B01,
- **S3C4520A** for ISDN / USB terminals,
- **S5N8946** for ADSL solutions,
- **S5N8947** a future enhanced version in the ADSL communications world.

1. S3C4510B01

- ♦ Architecture
  - ✓ Efficient and powerful **ARM7TDMI** core
  - ✓ Fully 32-bit RISC architecture
  - ✓ Little/Big-Endian mode supported basically, the internal architecture is big-endian. So, the little-endian mode only support for external memory.
  - ✓ Cost-effective JTAG-based debug solution
  - ✓ Boundary scan

- ♦ System Manager
  - ✓ **8/16/32-bit external bus** support for ROM/SRAM, Flash, DRAM EDO/normal or SDRAM, and external I/O
  - ✓ **8ko cache** configurable as an internal SRAM

- ♦ i2C Master mode controller

- ♦ Ethernet Controller
  - ✓ **100/10-Mbit** per second operation
  - ✓ Full compliance with IEEE standard 802.3
  - ✓ MII (Media Independent Interface) conforms to the ISO/IEC 802-3 and 7-wire 10-Mbps interface

- ♦ HDLCs to support two-channel serial communications.
  - ✓ Tx/Rx FIFOs have 8-word (8 × 32-bit) depth
  - ✓ Modem interface
  - ✓ **Up to 10 Mbps** operation

- ♦ 2 channels DMA Controller

- ♦ UARTs
  - ✓ 2 channels
  - ✓ Compliance with IrDA

- ♦ Others
  - ✓ 2 programmable 32-bit timers
  - ✓ 18 programmable I/O ports
  - ✓ 21 interrupt sources, including 4 external interrupt sources
  - ✓ Operating voltage range : **3.3 V** ± 5 %
  - ✓ Operating temperature range : 0 °C to + 70 °C
  - ✓ Operating frequency range : **up to 50 MHz with PLL built-in** (1:5 ratio)
  - ✓ Package type: **208-Pin QFP**

2. S3C4530A

This is an enhanced version of the S3C4510B01. The differences are focused on the improvement of UART characteristics. The added features are :

- ✓ High speed (460 Kbps) UART support with **32 byte Tx/Rx FIFO** and **modem interface signals**
- ✓ Automatic baud rate detection
- ✓ 8 control character comparison for software control
- ✓ Up to 26 programmable I/O (UART pins are shared with I/O pins)

3. S3C4520A

♦ Architecture

- ✓ Efficient and powerful **ARM7TDMI** core
- ✓ Fully 32-bit RISC architecture
- ✓ Little/Big-Endian mode supported basically, the internal architecture is big-endian. So, the little-endian mode only support for external memory.
- ✓ Cost-effective JTAG-based debug solution
- ✓ Boundary scan

♦ System Manager

- ✓ **8/16-bit external bus** support for ROM/SRAM, Flash, DRAM EDO/normal or SDRAM, and external I/O
- ✓ **4ko cache**

♦ 6 channels DMA Controller

♦ IOM-2 Controller

- ✓ IOM2 terminal mode support
- ✓ Inter device communication via IC channel
- ✓ TIC bus support
- ✓ Monitor channel collision control

♦ 3 channels HDLC Controller

- ✓ Tx and Rx FIFOs with 8 words (8*32-bit) depth
- ✓ Modem interface

♦ 3 Time Slot Assigner (TSA)

- ✓ To improve the flexibility of data path control between the 3 HDLCs and external interfaces

♦ UART

- ✓ 1 channel with 32 bytes FIFO for each Tx / Rx
- ✓ Up to 460 Kbps
- ✓ Hardware flow control, automatic baudrate selection
- ✓ Compliant with IrDA

♦ USB

- ✓ Compliant with USB 1.1 specifications
- ✓ Full speed 12 Mbps operation only with internal transceiver
- ✓ Support 5 Endpoints :
  1 Control (64 bytes FIFO),
  2 Interrupt (16 bytes FIFO),
  2 Data (64 bytes FIFO).

♦ Others

- ✓ 2 programmable 32-bit timers
- ✓ Watchdog
- ✓ 23 interrupt sources
- ✓ 38 programmable I/O ports (5V tolerant)
- ✓ **2 on-chip PLLs** : PLL0 for system clock and PLL1 for USB device
- ✓ Operating voltage range : **3.3 V** ± 5 %
- ✓ Operating temperature range : 0 °C to + 70 °C
- ✓ Operating frequency range : **up to 50 MHz with PLL built-in** (1:5 ratio)
- ✓ Package type: **144-Pin LQFP**

4. S5N8946

Main features :

- ✓ **4-Kbyte** unified cache
- ✓ SAR (Segmentation and Reassembly)
- ✓ **UTOPIA Level 1** Interface
- ✓ Ethernet MAC and **10Base-T** Transceiver
- ✓ **Full-rate USB** controller
- ✓ 2-CH GDMA (General Purpose Direct Memory Access)
- ✓ UART (Universal Asynchronous Receiver and Transmitter)
- ✓ 2 programmable 32bits Timers
- ✓ 18 Programmable I/O ports
- ✓ Interrupt controller
- ✓ **I2C** controller
- ✓ Built-in PLLs for System/USB
- ✓ Cost effective JTAG-based debug solution
- ✓ Boundary scan
- ✓ Operating Voltage Range : **3.3V**
- ✓ Operating Frequency Up to **50MHz**
- ✓ 240 QFP Package

5. S5N8947

This device will be available Q1-2002.

Main features :

- ✓ **4-Kbyte** unified cache
- ✓ SAR (Segmentation and Reassembly)
- ✓ **UTOPIA Level 2** Interface
- ✓ Ethernet MAC
- ✓ **Full-rate USB** controller
- ✓ 2-CH GDMA (General Purpose Direct Memory Access)
- ✓ UART (Universal Asynchronous Receiver and Transmtter)
- ✓ 2 programmable 32bits Timers
- ✓ 18 Programmable I/O ports
- ✓ Interrupt controller
- ✓ **I2C** controller
- ✓ Built-in PLLs for System/USB
- ✓ Cost effective JTAG-based debug solution
- ✓ Boundary scan
- ✓ Operating Voltage Range : **2.5V**
- ✓ Operating Frequency Up to **50MHz**
- ✓ 208 TQFP Package

III. EMBEDDED SOLUTIONS

A. Overview

This devices are designed to provide a cost-effective and high performance microcontroller solution for hand-held devices, power sensitive and general applications.

B. The offer

In this range, SAMSUNG is offering 3 mains devices :

- **S3C3410X** for an optimum performance/price ratio,
- **S3C44B0X** for high performances,
- **S3F441FX** for high integration.

1. **S3C3410X** : best performance/price ratio

♦ Architecture

- ✓ Efficient and powerful **ARM7TDMI** core
- ✓ Fully 32-bit RISC architecture
- ✓ Cost-effective JTAG-based debug solution

♦ System Manager

- ✓ **8/16-bit external bus** support for ROM/SRAM, Flash, DRAM EDO/normal or SDRAM, and external I/O
- ✓ 16 Mbytes address space for each 8 banks (Total 128 Mbytes)
- ✓ **4ko cache** configurable as an internal SRAM

♦ 2 channels DMA Controller

♦ 74 I/O ports (including the multiplexed I/O)

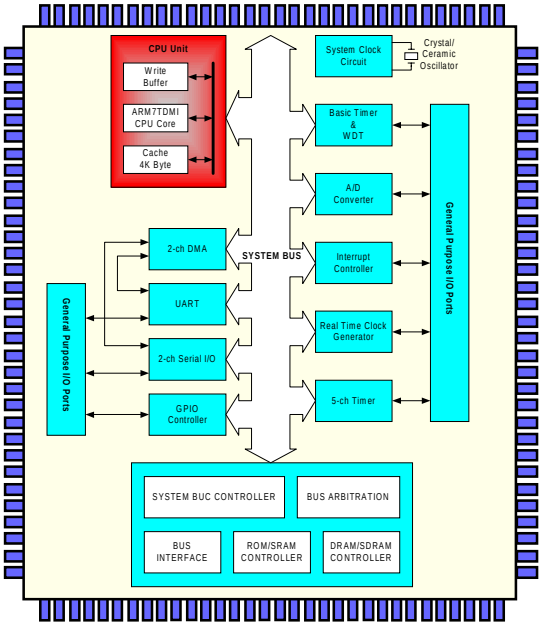
♦ Timers / Counters (3 x 16-bit + 8 x 8-bit)

♦ UART (1 channel) & SIO (2 channels)

♦ A/D Converter

- ✓ 8 channels
- ✓ **10-bit ADC**

♦ i2C Master mode controller



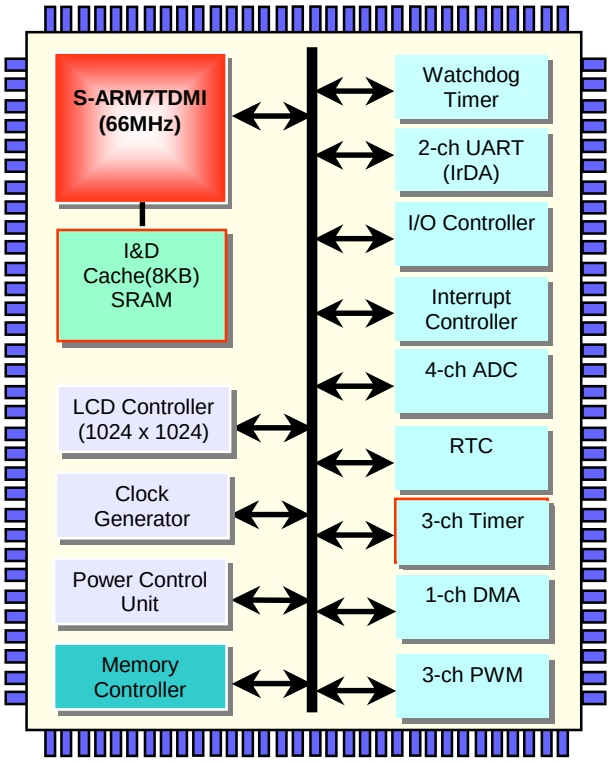
♦ RTC (Real Time Clock)

- ✓ 32.768 kHz operation (with 2nd external XTAL)
- ✓ **Full function** : seconds, minutes, hours, day, week, month, year.
- ✓ Alarm for CPU wake-up

♦ Others

- ✓ **Power down modes** : Idle, Slow (with programmable clock ratio) and Stop modes.
- ✓ Power consumption in Normal Mode : 1 to 2mA/MHz
- ✓ 35 interrupt sources, including 12 external interrupt sources.
- ✓ **Watchdog** and **Basic timer**
- ✓ Operating voltage range : **3.3 V** ± 5 %
- ✓ Operating temperature range : 0 °C to + 70 °C
- ✓ Operating frequency range : **up to 40 MHz**
- ✓ Package type : **128-Pin QFP**

2. S3C44B0X : high performances



♦ Architecture

- ✓ Efficient and powerful **ARM7TDMI** core
- ✓ Fully 32-bit RISC architecture
- ✓ Cost-effective JTAG-based debug solution
- ✓ 32x8 bit **hardware multiplier**
- ✓ High efficient architecture Bus

♦ System Manager

- ✓ **8/16/32-bit external bus** support for ROM/SRAM, Flash, DRAM EDO/normal or SDRAM, and external I/O
- ✓ 32 Mbytes address space for each 8 banks (Total 256 Mbytes)
- ✓ **8ko cache** configurable as an internal SRAM
- ✓ Little/big endian support

♦ UARTs

- ✓ 2 channels
- ✓ **32 bytes internal FIFO** for each Rx and Tx
- ✓ Support **hardware handshaking**
- ✓ Compliance with IrDA

♦ 1 channel SIO

♦ RTC (Real Time Clock)

- ✓ 32.768 kHz operation (with 2nd external XTAL)
- ✓ **Full function** : seconds, minutes, hours, day, week, month, year.
- ✓ Alarm for CPU wake-up
- ✓ Time tick interrupt

♦ 71 I/O ports (including the multiplexed I/O)

♦ 2 channels DMA Controller

♦ A/D Converter

- ✓ 8 channels
- ✓ **10-bit ADC**

♦ LCD controller

- ✓ Supports color (256 colors) / monochrome / gray (16 levels) LCD panel
- ✓ Supports single/dual scan displays
- ✓ Supports Multiple Virtual Display Screen. (Supports Hardware Horizontal/Vertical Scrolling)
- ✓ Dedicated DMA for fetching image data from system memory
- ✓ The system memory is used as the display memory
- ✓ Supports multiple screen size.
- ✓ Typical actual screen sizes: 640x480, 320x240, 160x160
- ✓ Maximum virtual screen sizes (color mode): 4096x1024, 2048x2048, 1024x4096, etc…

- i2C Master mode controller

- IIS Bus interface (Inter-IC Sound)
  - ✓ IIS, MSB-justified format compatible (to implement a CODEC interface to an external 8/16-bit stereo audio CODEC IC for mini-disc and portable applications)
  - ✓ Programmable frequency divider for master clock and CODEC clock
  - ✓ 32 bytes (2X16) FIFO for transmit and receive

- Timer with PWM (Pulse Width Modulation)
  - ✓ **6 channels**
  - ✓ PWM controller : programmable duty cycle, frequency and polarity.

- Others
  - ✓ **Power down modes** : Normal, idle, slow and stop modes.
  - ✓ 30 interrupt sources, including 8 external interrupt sources.
  - ✓ **Watchdog**
  - ✓ Operating voltage range : **3.3 V** ± 5 % (Core @ 2.5V)
  - ✓ Power consumption :

Normal Mode :	60mA typ. @ 66MHz
Idle Mode :	23mA typ. @ 66MHz
Slow Mode :	2.1mA typ. @ 1MHz
Stop Mode :	5µA typ.

  - ✓ Operating temperature range : 0° C to + 70° C
  - ✓ Operating frequency range : **up to 66 MHz with PLL built-in**
  - ✓ Package types : **160-Pin LQFP** / **160-Pin FBGA**

3. **S3F441FX** : high integration

♦ Architecture

- ✓ Efficient and powerful **ARM7TDMI** core
- ✓ Fully 32-bit RISC architecture
- ✓ Cost-effective JTAG-based debug solution
- ✓ **Built-in 256 Kbytes FLASH** memory (programmable via JTAG port)
- ✓ **8 Kbytes SRAM**

♦ System Manager

- ✓ **8-bit external bus**
- ✓ 3 external memory banks

♦ 1 channel UART

♦ Timers

- ✓ **6 x 16-bit** timer/counters
- ✓ Interval, capture or match & overflow mode operations

♦ Others

- ✓ **16 I/O Ports**
- ✓ **Power down modes** : Normal, idle and stop modes.
- ✓ 19 interrupt sources, including 3 external interrupt sources.
- ✓ **Watchdog** and **Basic timer**
- ✓ Operating voltage range : **3.3 V** ± 5 % (Core @ 2.5V)
- ✓ Power consumption :
  - Normal Mode : 29mA typ. @ 40MHz
  - Idle Mode : 4.8mA typ. @ 40MHz
  - Stop Mode : 5µA typ.
- ✓ Operating temperature range : 0° C to + 70° C
- ✓ Operating frequency range : **up to 40 MHz with PLL built-in**
- ✓ Package types : **64-Pin LQFP**

4. **S3C2400X** : come on into the race !

♦ Architecture

- ✓ **ARM920T** CPU core
- ✓ Fully 32-bit RISC and HARVARD based architecture
- ✓ Enhanced ARM architecture MMU to support WinCE, EPOC 32 and Linux
- ✓ Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- ✓ ARM920T CPU core supports the ARM debug architecture and has a Tracking ICE mode
- ✓ Internal Advanced Microcontroller Bus Architecture (**AMBA 2.0**, **AHB/APB**)

♦ System Manager

- ✓ **8/16/32-bit external bus** support for ROM/SRAM, Flash, DRAM EDO/normal or SDRAM, and external I/O
- ✓ 32M byte address space for each 8 banks (Total 256Mbytes)
- ✓ Little/Big Endian support
- ✓ **16KB Instruction-Cache** and **16KB Data-Cache**

♦ DMA Controller

- ✓ 4-ch DMA controller with Burst transfer mode

♦ Timer with PWM (Pulse Width Modulation)

- ✓ 4-ch 16-bit Timer with PWM + 1-ch 16-bit internal timer with DMA-based or interrupt-based operation

♦ UART

- ✓ 2-channel UART with DMA-based or interrupt-based operation
- ✓ Each channel has internal 16-byte Tx FIFO and 16-byte Rx FIFO
- ✓ Supports H/W handshaking during transmit/receive
- ✓ Programmable baud rate
- ✓ Supports IrDA 1.0

♦ A/D Converter

- ✓ 8-ch multiplexed **10-bit ADC**
- ✓ Up to 500KSPS

♦ LCD Controller

STN LCD displays Feature

- ✓ Supports 3 types of STN LCD panels : 4-bit dual scan, 4-bit single scan, 8-bit single scan display type.
- ✓ Supports the monochrome, 4 gray levels, 16 gray levels, 256 colors and 4096 colors
- ✓ Supports multiple screen size :
  - Typical actual screen size : 320x240, 160x160 (pixels)
  - Maximum virtual screen size (color mode) : 4096x1024, 2048x2048, 1024x4096 etc…
- ✓ Supports power saving mode (Enhanced SL_IDLE mode.)

TFT (Thin Film Transistor) color displays Feature

- ✓ Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT
- ✓ Supports 16 bpp non-palette true-color displays for color TFT
- ✓ Supports maximum 32K(64K using intensity) color TFT at 16 bpp mode
- ✓ Supports multiple screen size :
  - Recommended maximum screen size : 640x480 (8 bpp, 32bit SDRAM @80MHz)
  - Maximum virtual screen size (16 bpp mode) : 2048x1024 etc…

♦ IIC-BUS Interface

- ✓ 1-ch **Multi-Master IIC-Bus**
- ✓ Up to 400 Kbit/s

- ## IIS-BUS Interface
  - ✓ 1-ch IIS-bus for audio interface with DMA-based operation

- ## USB
  - ✓ **2-port USB Host + 1 port USB Device**
  - ✓ Complies with OHCI Rev. 1.0 for Host
  - ✓ 5 Endpoints for Device
  - ✓ Compatible with the USB Specification version 1.1

- ## MMC Interface
  - ✓ Multi-Media Card Protocol version 2.11 compatible
  - ✓ 2x16 Bytes FIFO for receive/transmit
  - ✓ DMA-based or interrupt-based operation

- ## SPI Interface
  - ✓ Serial Peripheral Interface Protocol version 2.11 compatible
  - ✓ 2x8 bits Shift register for receive/transmit
  - ✓ DMA-based or interrupt-based operation

- ## RTC (Real Time Clock)
  - ✓ **Full clock feature** : msec, sec, min, hour, day, week, month, year
  - ✓ 32.768 KHz operation
  - ✓ Alarm & Time tick interrupts

- ## Clock & Power Manager
  - ✓ Low power
  - ✓ **2 on-chip PLLs** :
    UPLL makes the clock for operating USB Host/Device.
    MPLL makes the clock for operating MCU at maximum 150Mhz @ 1.8V
  - ✓ Clock can be fed selectively to each function block by software
  - ✓ Power mode:

Normal mode :	Normal operating mode
Slow mode :	Low frequency clock without PLL
Idle mode :	Stop the clock for only CPU
Stop mode :	All clocks are stopped
SL_IDLE mode :	All clocks except LCD are stopped

  - ✓ Wake up by EINT[7:0] or RTC alarm interrupt from Stop mode.

- ## 90 multiplexed input/output ports

- ## Others
  - ✓ 32 Interrupt sources
    (Watch dog timer, 5 Timer, 6 UART, 8 External interrupts, 4 DMA, 2 RTC, 1 ADC, 1 IIC, 1 SPI, 1 MMC, 2 USB)
  - ✓ Watch-dog Timer
  - ✓ Operating Voltage Range :
    Core : 1.8V
    I/O : 3.3V
  - ✓ Operating Frequency : **Up to 150 Mhz**
  - ✓ Packages : **208 LQFP / 208 FBGA**

IV. OUTLINES

Reference	Architecture (external / internal @ max speed)	Application / Use	Evaluation Board
S3C4510B01	16 / 32 bits @ 50 MHz	Ethernet Appliances / Best performance/price ratio	KEB-50100
S3C4530A	32 / 32 bits @ 50 MHz	Ethernet Appliances / High performances	KEB-50300
S3C4520A	16 / 32 bits @ 50 MHz	ISDN TA - USB Modem router	N/A
S5N8946	32 / 32 bits @ 50 MHz	ADSL appliances	SCMDS-MCU
S5N8947	32 / 32 bits @ 50 MHz	ADSL appliances	N/A
S3C3410X	16 /32 bits @ 40 MHz	General Purpose / Best performance/price ratio	SMDK40100
S3C44B0X	32 / 32 bits @ 66 MHz	General Purpose with LCD / High performances	SMDK41100
S3F441FX	8 /32 bits @ 40 MHz	General Purpose with Flash/ High integration	SMDK40125
S3C2400X01	32/32 bits @ 150 MHz	Multimedia Appliances / Very High performances	N/A

All these devices are in Mass Production except :

- S5N8947 available in Q1-2002
- S3C2400X01 available in Q3-2001

V. VLINUX

vLinux is a tradmark of **Vitals System Inc**. for Embedded ARM Linux Solutions.
vLinux also can support Non-MMU ARM devices which are suitable for low cost design for commercial production

Vitals System Inc are providing vLinux solutions to customer as by consulting or professional engineering services under the service contract and NDA. We are release vLinux Service Package to customer as all source code format.

The size of the Vlinux ported to the Samsung ARM processor is about 3.0Mbytes (Full vLinux service packages) in size (Kernel : around 0.8Mbyte). It is possible to achieve a 40% compression ratio to 1.2Mbytes and decompress when booting from the BIOS to DRAM then the Kernel will start.

1. The samsung part and the demo board supported by Vlinux

The following solutions are suitable for Internet Access device like as Managed Hub/Switching Hub, ADSL/ISDN/Modem router, Printer Server , Web camera, Embedded Web Server …

Part	DemoBoard
S3C4510 (KS32C50100)	SNDS100
S3C4530 (KS32C50300)	NiBa

The following solutions are suitable for Internet Appliances like as PDA, Hand-Held device, eBook, GPS, Handy Game machine, Smart Phone etc.

Part	DemoBoard
S3C3410X (KS17C40100)	SMDK40100
S3C44B0X (KS32C41100)	SMDK41100

2. Training Pakage

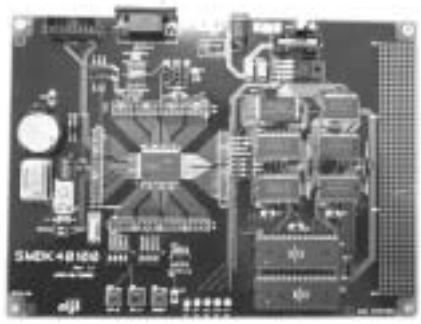
A training package is also available that contain BIOS, Kernel and applications which are all in vLinux service package are provided as binary image. Some network applications are also provided as source format. So, these applications can be built using GNU tool kits which also included in training kits. This package coul be run with the NiBa demo board.

Items	List	Descriptions	Comment
GNU Toolkits	**Bin Utilities**	• arm-elf-as : assembler • arm-elf-ld : linker • arm-elf-ar : library maker • arm-elf-addr2line • arm-elf-gasp • arm-elf-nm • arm-elf-objcopy • arm-elf-objdump • arm-elf-ranlib • arm-elf-readelf • arm-elf-run • arm-elf-size • arm-elf-strings • arm-elf-strip	
	Compiler	arm-elf-gcc : compiler	
	Utilities	elf2flt : flat binarary generation	
		genromfs: generate ROM file system	
Training Software Packages	**BIOS1.01**	This BIOS image include Serial (Y-Modem protocol) and network (TFTP) bootloader	
	Kernel	vLinux kernel (Linux kernel version 2.2.14) image	
	Library	libc : C libraries libm : Methmatical C libraries application C runtime 0 : Application entry points. application linker scripter	
Applications	**System utility**	Logname, hostname, login, init, expand , sysconf, shutdown, sync, uname, which, whoami, printenv, ps, kill, free	
	File utility	Cat, chgrp, chmod, chown, cmp, cp, dd, df, dirname, grep, ls, mkdir, mkfifo, mknod, rm , rmdir, more, touch, l, ln, mv	
	Shell utility	Sh, date, echo, pwd, basename	
	Inet utility	Inetd, ifconfig, route, ftp, ftpd, bootpc, telnet, Telnetd, thttpd, smtp, discard, pppd, htpasswd	
	Mount with NFS	Mount, umount	
	Editor	EE(easy editor)	
	etc	Memory Dump function	
	TFTP	TFTP client program	***Note**
	HTTPD	Simple HTTP Server	
	Ping	PING application	
	CGI-SRC	CGI test source program	
	Debug	Memory dump	
	User Application	rtc.c for Realtime clock control lcd.c for LCD display	
Diagnostic code		Diagnostic code for debuging board functions	
		system initialize assembler download via xy-modem protocol some of low level diagnostic	
Documents	**Manual**	vLinux Training Kits User Manual	

Note : These items are provided to customer as source code format.

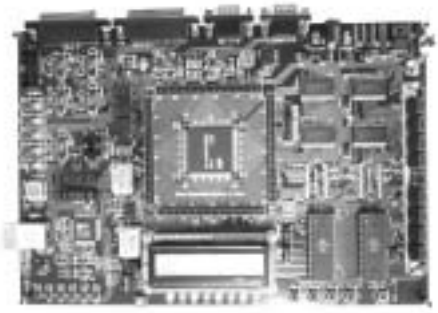
3. Reference Board Features

SMDK40100 (Evaluation Board for S3C3410)



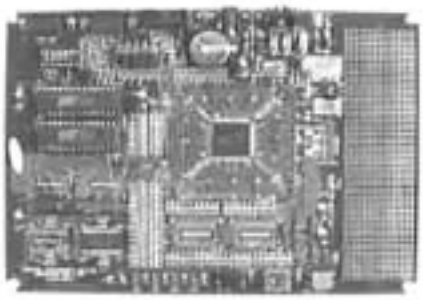
- Processor : S3C3410 (ARM7TDMI)
- Boot ROM : One mounted Flash Memory, two socket (accept up to 8Mbit)
- RAM : One SRAM with 256K x 16bit
- Two SDRAMs & Two EDODRAMs (8M)
- Real Time Clock (32.768Khz)
- One serial Port for console
- One JTAG Port
- Four extendable connector
- Five LED indicators
- Three switch for system reset and external interrupt

SNDS100 (Evaluation Board for S3C4510X/B)



- Processor: S3C4510 (ARM7TDMI)
- Boot ROM : Up to 8Mbit, support byte, half-word & word size boot ROM
- DRAM : 72-pin SIMM module with two banks EDO DRAM support
- External I/O : status LCM driver.
- General I/O : control switches and status display LED
- Two serial ports, one for console
- IIC-bus EEPROM
- Two channel serial communication interface.
- 10/100Mbds Ethernet interface
- Provides source code for example programs which use the peripheral

SMDK41100(Evaluation Board for S3C44B0)



- Processor: S3C44B0 (ARM7TDMI)
- Boot ROM : Up to 8Mbit, support byte, half-word size boot ROM
- DRAM : Two 4M x 16 SDRAM support
- General I/O : control switches and status display LED
- Two serial ports, one for console
- Graphic LCM interface
- Provides power supply for LCM
- IIC-bus EEPROM
- Supports sub clock 32768Hz crystal
- Provides back battery
- Provides source code for example programs which use the peripheral

SCMDS-MCU-Rev1.0 (Evaluation Board for S5N8946)

Hardware support :
- Evaluation Board
- Samples
- Schematic & BOM

Software support
- RTOS BSP : pSOS, Nucleus, Precise,vLinux
- Diagnostic Program including Low level Driver

VI. RTOS

The Samsung parts support Real Time Operating System like

- pSOS
- Nucleus
- VxWorks 5.4

VII. WEB SHORT CUT

On the Samsung Web, you will found differents information like:

- User Manual, schematic, demoboard, source codes, application notes …

http://samsungelectronics.com/semiconductors/System_LSI/32_bit_ARM_based_RISC_MPU/Network/S3C4510B/s3c4510b.htm
http://samsungelectronics.com/semiconductors/System_LSI/32_bit_ARM_based_RISC_MPU/Network/S3C4530A/s3c4530a.htm
http://samsungelectronics.com/semiconductors/System_LSI/32_bit_ARM_based_RISC_MPU/PDA/S3C3410X/s3c3410x.htm
http://samsungelectronics.com/semiconductors/System_LSI/32_bit_ARM_based_RISC_MPU/PDA/S3C44B0X/s3c44b0x.htm
http://samsungelectronics.com/semiconductors/System_LSI/32_bit_ARM_based_RISC_MPU/HDD/S3F441FX/s3f441fx.htm

VIII. WEB @

SAMSUNG	**http://www.samsungsemi.com**
ARM	**http://www.arm.com**
WBC	**http://www.wbc-europe.com**
Vital System Inc	**http://www.vitals.co.kr**
	http://www.armlinux.net
JEENI	**http://www.episupport.com**
pSOS	**http://www.isi.com**
Nucleus	**http://www.atinucleus.com**
VxWorks	**http://www.wrs.com**